The following Listing of the Claims will replace all prior versions and listings of the claims in this application:

Listing of the Claims

1. (Original) A switch router circuit comprising:

a plurality of Media Access Control (MAC) units, each MAC unit connected to a data bus for receiving incoming data packets from the data bus, each incoming data packet including a packet header and a packet payload, the packet header identifying a destination port to which the packet payload is to be transferred;

a controller connected to the MAC units to receive the incoming data packets therefrom, and wherein, for each incoming data packet, the controller separates the packet header of said data packet from the packet payload of said data packet;

a lookup table connected to the controller to receive packet headers therefrom, and wherein the lookup table utilizes a packet header to determine whether the destination port identified by said packet header is include within the plurality of MAC units of said switch router circuit;

a multi-port store/switch memory array connected to receive packet payloads of incoming data packets, the multi-port store/switch memory array including a plurality of storage areas, each storage area being associated with a corresponding MAC unit such that a packet payload of an incoming data packet received by a MAC unit is stored in the corresponding storage area of the multi-port store/switch memory array; and

an arbitrator connected to the multi-port store/switch memory array, and wherein the arbitrator, in the event that the destination port identified by the packet header of an incoming data packet is included within the plurality of MAC units of said switch/router circuit, arbitrates direct connection of the memory array storage area associated with the MAC unit that receives the incoming data packet to the MAC unit identified as the destination port, thereby facilitating direct transfer of the packet payload of the incoming data packet to the destination port.

2. (Original) A switch router circuit as in claim 1, and wherein each of the storage areas in the multi-port store/switch memory array includes a plurality of pass gates, one pass gate being associated with a corresponding one of the MAC units, and wherein each of the plurality of storage areas further includes a data storage element, such that the arbitrator arbitrates the pass gates of the incoming storage area to the pass gates of the outgoing storage area, whereby the packet payload is transferred directly from the data storage element of the incoming storage area to the date storage element of the outgoing storage area.

3. (Original) A switch router circuit as in claim 1, and wherein the arbitrator arbitrates direct connection of the memory array storage area associated with the MAC unit that receives the incoming data packet to multiple MAC units identified as destination ports, thereby facilitating multicasting of the packet payload to the multiple destination ports.

4. (Original) A switch router circuit as in claim 1, and wherein the multi-port store/switch memory array facilitates double ended write of incoming packet payloads and buffered multi-port read of outgoing packet payloads.

5. (Original) A switch router circuit as in claim 1, and wherein the multi-port store/switch memory array facilitates double port write of incoming packet payloads and buffered double port read of outgoing packet payloads.